Dame, that implements a Hartree-Fock mathematical model of the physics of a QCA array. The simulation was performed for an assumed cell size of 20 nm and inter-cell distance of 14 nm.

The results of the simulation showed that for a basic QCA majority gate, an output error would occur if the errors in the relative positions of adjacent cells were to exceed various amounts of the order of the size of a cell or a significant fraction thereof (the exact amounts being different for different cells and different directions of displacement). In the case of a molecular implementation, this would translate to a requirement for impractical sub-nanometer manufacturing tolerances. On the other hand, the simulation showed that even with errors as large as those depicted for the block majority gate at the bottom of the figure, there would be no output error.

This work was done by Amir Firjany, Nikzad Toomarian, and Katayoon Modarres of Caltech for **NASA's Jet Propulsion Laboratory**. *Further information is contained in a TSP (see Page 1).*

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Hybrid VLSI/QCA Architecture for Computing FFTs

Simplification is effected through use of QCA circuitry to permute data.

NASA's Jet Propulsion Laboratory, Pasadena, California

A data-processor architecture that would incorporate elements of both conventional very-large-scale integrated (VLSI) circuitry and quantum-dot cellular automata (QCA) has been proposed to enable the highly parallel and systolic computation of fast Fourier transforms (FFTs). The proposed circuit would complement the QCA-based circuits described in several prior *NASA Tech Briefs* articles, namely "Implementing Permutation Matrices by Use of Quantum Dots" (NPO-20801), Vol. 25, No. 10 (October 2001), page 42; "Compact Interconnection Networks Based on Quantum Dots" (NPO-20855) Vol. 27, No. 1 (January 2003), page 32; and "Bit-Serial Adder Based on Quantum Dots" (NPO-20869), Vol. 27, No. 1 (January 2003), page 35.

The cited prior articles described the limitations of very-large-scale integrated (VLSI) circuitry and the major potential advantage afforded by QCA. To recapitulate: In a VLSI circuit, signal paths that are required not to interact with each other must not cross in the same plane. In contrast, for reasons too complex to describe in the limited space available for this article, suitably designed and operated QCA-based signal paths that are required not to interact with each other can nevertheless be allowed to cross each other in the same plane without adverse effect. In principle, this characteristic could be exploited to design compact, coplanar, simple (relative to VLSI) QCA-based networks to implement complex, advanced interconnection schemes.

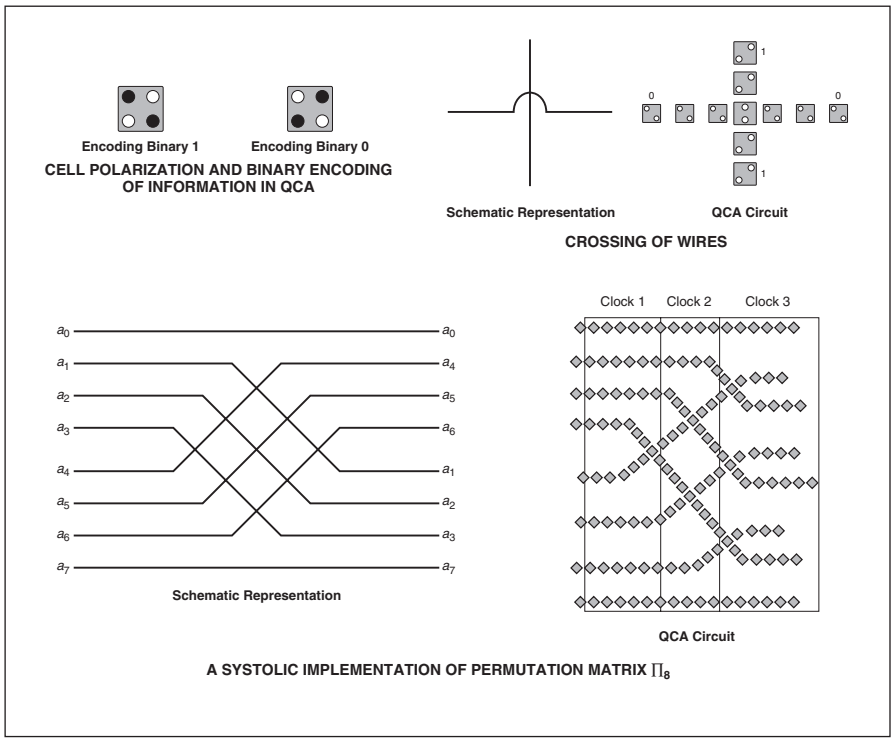

Figure 1. **QCA Are Assembled Into Binary Wires,** and the wires are patterned to implement a perfect-shuffle permutation matrix known as Π_8.

To enable a meaningful description of the proposed FFT-processor architecture, it is necessary to further recapitulate the description of a quantum-dot cellular automaton from the first-mentioned prior article: A quantum-dot cellular automaton contains four quantum dots positioned at or between the corners of a square cell. The cell contains two extra mobile electrons that can tunnel (in the quantum-mechanical sense) between neighboring dots within the cell. The Coulomb repulsion between the two electrons tends to make them occupy antipodal dots in the cell. For an isolated cell, there are two energetically equivalent arrangements (denoted polarization states) of the extra electrons. The cell polarization is used to encode binary information. Because the polarization of a nonisolated cell depends on Coulomb-repulsion interactions with neighboring cells, universal logic gates

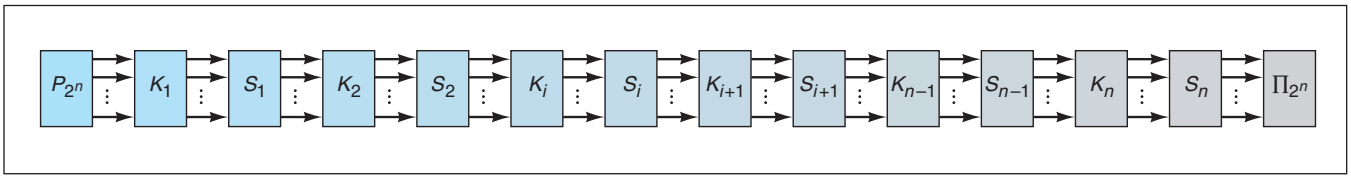

Figure 2. A **Hybrid of VLSI and QCA Circuit Modules** would perform a parallel, systolic computation of an FFT. The particular circuit architecture is based on a matrix factorization of the FFT.

and binary wires could be constructed, in principle, by arraying QCA of suitable design in suitable patterns.

Again, for reasons too complex to describe here, in order to ensure accuracy and timeliness of the output of a QCA array, it is necessary to resort to an adiabatic switching scheme in which the QCA array is divided into subarrays, each controlled by a different phase of a multiphase clock signal. In this scheme, each subarray is given time to perform its computation, then its state is frozen by raising its interdot potential barriers and its output is fed as the input to the successor subarray. The successor subarray is kept in an unpolarized state so it does not influence the calculation of preceding subarray. Such a clocking scheme is consistent with pipeline computation in the sense that each different subarray can perform a different part of an overall computation. In other words, QCA arrays are inherently suitable for pipeline and, moreover, systolic computations. This sequential or pipeline aspect of QCA would be utilized in the proposed FFT-processor architecture.

Heretofore, the main obstacle to designing VLSI circuits for systolic and highly parallel computation of FFTs (and of other fast transforms commonly used in the processing of images and signals) has been the need for complex data permutations that cannot be implemented without crossing of signal paths. The proposed hybrid VLSI/QCA FFT-processor architecture would exploit the coplanar-signal-path-crossing capability of QCA to implement the various permutations directly in patterns of binary wires (that is, linear arrays of quantum dots), as in the example of Figure 1. The proposed architecture is based on a reformulation of the FFT by use of a particular matrix factorization that is suitable for systolic implementation. The reformulated FFT is given by

$$F_{2^n} = \Pi_{2^n} S_n K_n S_{n-1} K_{n-1} \cdots S_{i+1} K_{i+1} S_i K_i \cdots S_2 K_2 S_1 K_1 P_{2^n},$$

where n is an integer; F_{2^n} is a radix-2 FFT for a 2^n-dimensional vector; Π_{2^n}, S_i (where i is an integer), and P_{2^n} are various permutation operators or matrices; and the K_i are arithmetic operators.

Figure 2 depicts the proposed architecture. The permutation operators would be implemented by QCA modules, while the arithmetic operators K_i would be implemented by VLSI modules containing simple bit-serial processing elements. Each processing element would receive input data from two sources and would produce two outputs by performing simple multiplication and addition operations. Aside from being driven by the same clock (in order to obtain the necessary global synchronization), the processing elements would operate independently of each other; because of this feature, the processing modules would be amenable to large-scale implementation in complementary metal oxide/semiconductor (CMOS) VLSI circuitry. To obtain the necessary global synchronization, the VLSI and the QCA modules would be driven by the same clock.

This work was done by Amir Fijany, Nikzad Toomarian, Katayoon Modarres, and Matthew Spotnitz of Caltech for **NASA's Jet Propulsion Laboratory**. *Further information is contained in a TSP (see page 1).* *NPO-20923*

Arrays of Carbon Nanotubes as RF Filters in Waveguides

Advantages would include compactness and high Q.

NASA's Jet Propulsion Laboratory, Pasadena, California

Brushlike arrays of carbon nanotubes embedded in microstrip waveguides provide highly efficient (high-Q) mechanical resonators that will enable ultraminiature radio-frequency (RF) integrated circuits. In its basic form, this invention is an RF filter based on a carbon nanotube array embedded in a microstrip (or coplanar) waveguide, as shown in Figure 1. In addition, arrays of these nanotube-based RF filters can be used as an RF filter bank.

Applications of this new nanotube array device include a variety of communications and signal-processing technologies. High-Q resonators are essential for stable, low-noise communications, and radar applications. Mechanical oscillators can exhibit orders of magnitude higher Qs than electronic resonant circuits, which are limited by resistive losses. This has motivated the development of a variety of mechanical resonators, including bulk acoustic wave (BAW) resonators, surface acoustic wave (SAW) resonators, and Si and SiC micromachined resonators (known as "microelectromechanical systems" or MEMS). There is also a strong push to extend the resonant frequencies of these oscillators into the GHz regime of state-of-the-art electronics. Unfortunately, the BAW and

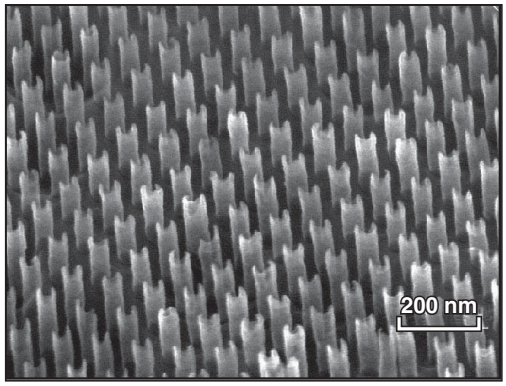

Figure 1. This **Array of Carbon Nanotubes**, with a diameter nonuniformity of <5 percent, was fabricated in a process that included the use of a nanopore template (J. Xu et al.).